IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Tsecouras	Docket No:	TI-33116
Serial No:	10/068,492	Examiner:	Le, Duy K
Filed:	2/5/2002	Art Unit:	2685
For:	ADAPTIVE PULSE FRAME RATE FREQUENCY CONTROL FOR DIGITAL AMPLIFIER SYSTEMS		

APPEAL BRIEF PURSUANT TO 1.192(c)

CERTIFICATION OF FACSIMILE TRANSMISSION

I hereby certify that the following papers are being transmitted by facsimile to the U.S. Patent and Trademark Office at 571-273-8300 on 1-30-06

Tommie Chambers

Assistant Commissioner for Patents
Washington, DC 20231

Dear Sir:

The following Appeal Brief is respectfully submitted in connection with the above identified application in response to the final Office Action mailed June 2, 2005, and the Advisory Action mailed November 29, 2005.

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated.

RELATED APPEALS AND INTERFERENCES

Appellants legal representative knows of no appeals or interferences which will be directly affected, or have a bearing on the Board's decision.

STATUS OF THE CLAIMS

Claims 1-29 were originally filed and no claims have been cancelled or added.

Consequently, the subject matter of the instant appeal is the final rejection of Claims 1-29.

STATUS OF AMENDMENTS

The application was originally filed with Claims 1-29.

A Response After Final was mailed on September 14, 2005, amending no claims.

The Advisory Action indicated that the Request for Consideration had been considered.

SUMMARY OF THE CLAIMED SUBJECT MATTER

Figure 1 is a high level block diagram illustrating one embodiment of the present adaptive pulse frame rate frequency control process 100. The process 100 commences when a user provides frequency information via a user interface such as a keypad 102 to a controller 104. The controller 104 can be a computer or otherwise include a data processing device such as a CPU, micro-controller, DSP, or other device capable of processing the user selected frequency information. The controller 104 can include a look-up table 106 of frequencies or an algorithm 108 capable of calculating the proper pulse frame frequency in response to the user selected frequency information. The look-up table 106 of frequencies (e.g., desired pulse frame frequencies) versus AM/FM/TV stations desired for listening/recording can be constructed to minimize interference in the keep-out bands for the frequencies related to the source selected. The look-up table 106 most preferably contains desired pulse frame frequencies in which neither the pulse frame frequency nor its harmonics

(including the span frequencies related to the bandwidth of the information) can be either multiples or sub-multiples of the AM/FM/TV band frequencies as selected by the user. As stated herein before, selection of the programmed pulse frame frequency(s), the frequency multiple(s) and sub-multiple(s) should also not interfere with the IF and LCO as required by the receiver type selected. After processing the user selected frequency information, the controller 104 generates the requisite output control data bits 110 for proper pulse-frame frequency selection. The output control data bits 110 are then communicated to a decoder 112 to generate the requisite control data. Thus, when the user selects a given station on the AM/FM/TV band, the controller 104 commences to retrieve the proper pulse frame rate that will not interfere with the frequencies of the selected program material. The controller 104 updates a digital asynchronous sample rate converter master clock generator 114 using the control data generated via decoder 112 to obtain the new proper pulse-frame frequency selection. The digital asynchronous sample rate converter master clock generator 114 continues to output this frequency until the user selects another source. At that point, the controller 104 again retrieves the proper pulse frame rate that will not interfere with the frequencies of the newly selected program material. The controller 104 updates the digital asynchronous sample rate converter master clock generator 114 with the newest values necessary to obtain the newest proper pulse-frame frequency selection. Each time another selection is made, the look-up table 106 is retrieved, and/or the algorithm 108 is set into operation, and a correct digital asynchronous sample rate converter master clock generator 114 frequency is selected.

Looking now at Figure 2, a simplified block diagram illustrates an adaptive pulse frame rate frequency controlled digital amplifier system 200 suitable for use with the digital asynchronous sample rate converter master clock generation scheme 100 depicted in Figure 1 according to one embodiment of the present invention. The digital amplifier system 200 importantly can be seen to employ a digital asynchronous sample rate converter 202. Such sample rate converters are well known to those skilled in the sample rate converter art, and so specific details regarding the operating characteristics of the sample rate converter 202 will not be discussed herein to better preserve clarity and brevity. It is well known to those skilled in the sample rate conversion art, for

example, to implement sample rate conversion in a hybrid digital/analog domain using a digital-to-analog (D/A) converter followed by an analog-to-digital (A/D) converter. The D/A converter runs at the input sample rate while the A/D converter is controlled by the output sample rate. If the output sample rate is lower, an analog anti-aliasing filter is provided between them. Performing sample rate conversion in the digital domain has been a research/development topic for more than a decade. The article by R.E. Crochiere and L.R. Rabiner, "Interpolation and decimation of digital signals-A tutorial review," *Proc.* IEEE, vol. 69, pp. 300-331, March 1981, is an excellent reference for understanding fundamental insights from early research results in the art area. The present invention is not so limited however; and it is anticipated that the present invention may also be implemented using appropriate analog-to-digital (ADC) sample rate conversion techniques that do not require first converting a digital input signal to an analog signal. Such an implementation may, for example, simply employ an ADC to process an analog input signal provided directly by an external device. The processed signal could then be communicated to a data processing device such as a computer, CPU, micro-controller, digital signal processor (DSP), or other appropriate data processing device to alter the sample rate of the signal that is ultimately passed on to the digital amplifier system. With continued reference now to Figure 2, the digital asynchronous sample rate converter 202 depicted in the adaptive pulse frame rate frequency controlled digital amplifier system embodiment 200 receives input audio data 203 as well as input audio clocks 205 in a manner also well-known to those skilled in the digital asynchronous sample rate converter art. The digital asynchronous sample rate converter master clock generator 114 discussed herein before is most preferably implemented using, for example, either a digital frequency synthesizer 207 or a programmable phase locked loop 209 such as depicted in Figure 2. The present invention is not so limited however, and it will be appreciated by those skilled in the art that any means can be used to generate the digital asynchronous sample rate converter master clock 114 so long as it is programmable via the output control data bits 110 to achieve proper selection of the desired pulse-frame frequency. The controller 104 generates the requisite output control data bits 110 necessary for the digital frequency synthesizer 207 or programmable phase locked loop 209 to generate

the system clocks 211 associated with the digital asynchronous sample rate converter 202 and the digital amplifier 204 portion of the system 200. The digital asynchronous sample rate converter 202 is then re-clocked via the system clocks 211 to output audio data at a new proper sample rate constructed to minimize interference in the keep-out bands for the frequencies related to the source selected as stated herein before. Similarly, the digital amplifier 204 is also re-clocked using audio clocks at the new sample rate. The digital amplifier 204 then processes the audio data and the audio clocks at the new sample rate to switch its output at the new pulse-frame rate in response to the AM/FM/TV band frequency data selected by the user such as discussed herein before. The output signal from the digital amplifier 204 is then passed through an appropriate filter 206 into a loudspeaker 208 such that critical frequency band interference caused by EMI generally associated with the digital switching amplifier 204 is avoided.

GROUNDS OF REJECTION

The two issues on appeal are first whether Claims 1-5, 11-15, 18-21, 24, 25, 28, and 29 are unpatentable under 35 U.S.C. § 103 over Matsushita in view of Orndorff; and secondly whether Claims 6-10, 16, 17, 22, 23, 26, and 27 are unpatentable under 35 U.S.C. § 103 over Matsushita in view of Orndorff and further in view of Midya.

ARGUMENTS

Matsushita does not disclose or suggest the presently claimed invention including a programmable controller operational in response to user selected frequency data to generate control data bits in independent Claim 1, the programmable controller operational in response to user selected frequency information to generate control data bits in independent Claim 12, the programmable programming means for generating control data bits in response to user selected input frequency information in independent Claim 18, albeit defined as the method step of communicating user selected input

frequency data to the controller such that the controller generates control data bits determined by the user selected input frequency data in independent Claim 25.

Applicants agree with the Examiner that Matsushita does not disclose this aspect.

It is respectfully submitted that Orndorff does not disclose or suggest the presently claimed invention including the programmable controller operational in response to the user selected input frequency data to generate control data bits in the various forms in independent Claims 1, 12, 18, and 25.

The Examiner alleges that Orndorff discloses a programmable controller operational in response to user selected input data to generate control data bits.

Notwithstanding the allegations of the Examiner, the Examiner's attention is directed to column 3, lines 9-15 where Orndorff discloses that Figure 3 illustrates the meter circuitry in block diagram form. The above described function key 16 and spin knob 14 provide inputs to the microcontroller 30 which, among other things as will be described, provides control signals to a three-stage attenuator and the first and second local oscillator phased-lock loop ICs 34 and 36.

Nothing in this part of the disclosure does Orndorff relate to frequency. Orndorff does not describe the function of key 16 or spin knob 14 in terms of the function that they provide.

The receive spurs or the look-up tables are not user selected.

The Examiner alleges that the "selection of frequency is performed on a look-up table set by the user" in the Office Action mailed June 2, 2005, page 12, middle of the page.

No look-up table is disclosed.

A EPPROM is disclosed but the information stored is not user selected.

Midya does not cure the above noted defects.

CONCLUSION

For the foregoing reasons, Appellants respectfully submit that the Examiner's final rejection of Claims 1-29 under 35 U.S.C. § 103 is not properly founded in law, and it is respectfully requested that the Board of Patent Appeals and Interferences so find and reverse the Examiner's rejections.

To the extent necessary, the Appellants petition for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,

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APPENDIX

1. A digital amplifier adaptive pulse frame rate frequency control system comprising:

a sample rate converter;

a programmable controller operational in response to user selected input frequency data to generate control data bits; and

a system clock generator operational to generate a sample rate converter master clock signal in response to the control data bits such that the sample rate converter generates output data at a sample rate determined by the control data bits.

2. The digital amplifier adaptive pulse frame rate frequency control system according to claim 1 wherein the programmable controller comprises a data processing device selected from the group consisting of a computer, a digital signal processor (DSP), a CPU, and a micro-controller.

3. The digital amplifier adaptive pulse frame rate frequency control system according to claim 1 wherein the system clock generator comprises a frequency controller selected from the group consisting of a digital frequency synthesizer, and a programmable phase-locked loop.

4. The digital amplifier adaptive pulse frame rate frequency control system according to claim 1 wherein the system clock generator is further operational to generate audio clock signals at the sample rate determined by the control data bits.

5. The digital amplifier adaptive pulse frame rate frequency control system according to claim 4 wherein the system clock generator is further operational to generate sample clock signals at the sample rate determined by the control data bits.

6. The digital amplifier adaptive pulse frame rate frequency control system according to claim 4 further comprising a digital amplifier responsive to the system clock generator audio clock signals and the sample rate converter output data such that the digital amplifier output switches at a pulse-frame rate determined by the system clock generator audio clock signals and the sample rate converter output data.

7. The digital amplifier adaptive pulse frame rate frequency control system according to claim 6 wherein the digital amplifier output further switches at a pulse-frame rate to minimize interference associated with keep-out bands for frequencies related to a desired source.

8. The digital amplifier adaptive pulse frame rate frequency control system according to claim 7 wherein the keep-out bands are associated with frequencies selected from the group consisting of AM, FM and TV band frequencies.

9. The digital amplifier adaptive pulse frame rate frequency control system according to claim 7 wherein the keep-out bands are associated with frequencies selected from the group consisting of radio frequency (RF), intermediate frequency (IF), and Local Control Oscillator (LCO) frequencies.

10. The digital amplifier adaptive pulse frame rate frequency control system according to claim 7 wherein the keep-out bands are associated with wireless

communication frequencies selected from the group consisting of cellular telephone frequencies and Bluetooth frequencies.

11. The digital amplifier adaptive pulse frame rate frequency control system according to claim 1 wherein the sample rate converter comprises a digital asynchronous sample rate converter.

12. A digital amplifier adaptive pulse frame rate frequency control system comprising:

a digital asynchronous sample rate converter operational to generate output audio data in response to input audio data, an input audio clock and a master clock;

a programmable controller operational in response to user selected input frequency information to generate control data bits, wherein the input frequency information is selected from the group consisting of wireless, cellular telephone, Bluetooth, RF, IF, LCO, AM, FM, and TV band frequencies;

a decoder operational to decode the control data bits; and

a system clock generator operational to generate the master clock in response to the decoded control data bits such that the digital asynchronous sample rate converter generates the output data at a sample rate determined by the user selected input frequency information.

13. The digital amplifier adaptive pulse frame rate frequency control system according to claim 12 wherein the programmable controller comprises a data processing device selected from the group consisting of a computer, a DSP, a CPU, and a micro-controller.

14. The digital amplifier adaptive pulse frame rate frequency control system according to claim 12 wherein the system clock generator comprises a frequency controller selected from the group consisting of a digital frequency synthesizer, and a programmable phase-locked loop.

15. The digital amplifier adaptive pulse frame rate frequency control system according to claim 12 wherein the system clock generator is further operational to generate audio clocks at the sample rate determined by the user selected input frequency information.

16. The digital amplifier adaptive pulse frame rate frequency control system according to claim 15 further comprising a digital amplifier responsive to the system clock generator audio clocks and the digital asynchronous sample rate converter output audio data such that the digital amplifier output switches at a pulse-frame rate determined by the user selected input frequency information.

17. The digital amplifier adaptive pulse frame rate frequency control system according to claim 16 wherein the digital amplifier output switches at a pulse-frame rate to minimize interference with keep-out bands associated with the input frequency information.

18. A digital amplifier adaptive pulse frame rate frequency control system comprising:

digital asynchronous sample rate converting means for generating output audio data in response to input audio data, an input audio clock and a master clock;

programmable controlling means for generating control data bits in response to user selected input frequency information, wherein the input frequency information is selected from the group consisting of RF, IF, LCO, AM, FM, TV, wireless, cellular telephone and Bluetooth band frequencies;

decoding means for decoding the control data bits; and

clock generating means for generating the master clock in response to the decoded control data bits such that the digital asynchronous sample rate converting means generates the output data at a sample rate determined by the user selected input frequency information.

19. The digital amplifier adaptive pulse frame rate frequency control system according to claim 18 wherein the programmable controlling means comprises a data processing device selected from the group consisting of a computer, a DSP, a CPU, and a micro-controller.

20. The digital amplifier adaptive pulse frame rate frequency control system according to claim 18 wherein the clock generating means comprises a frequency controller selected from the group consisting of a digital frequency synthesizer, and a programmable phase-locked loop.

21. The digital amplifier adaptive pulse frame rate frequency control system according to claim 18 wherein the clock generating means is further operational to generate audio clocks at the sample rate determined by the user selected input frequency information.

22. The digital amplifier adaptive pulse frame rate frequency control system according to claim 21 further comprising a digital amplifying means for generating an output signal that switches at a pulse-frame rate determined by the user selected input frequency information in response to the clock generating means audio clocks and the digital asynchronous sample rate converting means output audio data.

23. The digital amplifier adaptive pulse frame rate frequency control system according to claim 22 wherein the digital amplifying means output signal further switches at a pulse-frame rate that minimizes interference with keep-out bands associated with input frequency information.

24. The digital amplifier adaptive pulse frame rate frequency control system according to claim 18 wherein the clock generating means is further operational to generate sample clocks at the sample rate determined by the user selected input frequency information.

25. A method of controlling the pulse-frame rates for a digital amplifier output signal comprising the steps of:

providing a pulse-frame rate frequency control system having a programmable controller, a system clock generator, and a digital asynchronous sample rate converter operational to generate output audio data at a first sample rate in response to input audio data and further in response to input audio clocks;

communicating user selected input frequency data to the controller such that the controller generates control data bits determined by the user selected input frequency data;

communicating the control data bits to the system clock such that the system clock generates a master clock for the digital asynchronous sample rate converter at a

new sample rate and further such that the system clock generates output audio clocks at the new sample rate; and

adapting the digital asynchronous sample rate converter output audio data at a first sample rate to conform to the new sample rate determined by the master clock.

26. The method according to claim 25 further comprising the steps of:

providing a digital amplifier having output switching responsive to the digital asynchronous sample rate converter output audio data and further responsive to the output audio clocks at the new sample rate; and

communicating the digital asynchronous sample rate converter output audio data and the output audio clocks at the new sample rate to the digital amplifier such that the digital amplifier operates to change its output switching pulse-frame rate from a first pulse-frame rate to new pulse-frame rate.

27. The method according to claim 25 further comprising the steps of:

providing a digital amplifier having output switching responsive to the digital asynchronous sample rate converter output audio data and further responsive to the output audio clocks at the new sample rate; and

communicating the digital asynchronous sample rate converter output audio data and the output audio clocks at the new sample rate to the digital amplifier such that the digital amplifier operates to change its output switching pulse-frame rate to a new pulse-frame rate that substantially minimizes interference minimizes interference with keep-out bands associated with the frequency group consisting of AM, FM, and TV band frequencies.

28. The method of claim 25 wherein the step of communicating user selected input frequency data to the controller such that the controller generates control data bits determined by the user selected input frequency data comprises the step of providing a look-up table of pulse-frame frequencies (output digital asynchronous sample rate converter clock generator frequencies) versus station data selected from the group consisting of RF, IF, LCO, AM, FM, TV station, wireless, cellular telephone and Bluetooth frequencies, that can be accessed by the controller to determine the control data bits.

29. The method of claim 25 wherein the step of communicating user selected input frequency data to the controller such that the controller generates control data bits determined by the user selected input frequency data comprises the step of providing an algorithm to select pulse-frame frequencies (output digital asynchronous sample rate converter clock generator frequencies) versus station data selected from the group consisting of RF, IF, LCO, AM, FM, TV station, wireless, cellular telephone and Bluetooth frequencies, that can be accessed by the controller to determine the control data bits.

EVIDENCE APPENDIX

Appellants are submitting no items of evidence.

RELATED PROCEEDINGS APPENDIX

Appellants have no submission for the Related Proceeding Appendix.